Embedded Crew Interface and Display System for Gaganyaan Mission

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***Abstract*— One of the important elements in Human spaceflight is the technology required to enable humans to interact, monitor and control various onboard systems and provide them with essential information. To cater to this requirement for the Gaganyaan mission, a Crew Interface and Display System (CIDS) system based on an embedded SoC (System on Chip) has been developed at SAC/ISRO. This paper elaborates the key features, hardware-software architecture, environmental characterization and test results of the realized CIDS. This compact, reliable and versatile system weighs approximately 2.0 Kgs and dissipates less than 15 watts of power under nominal conditions.**

***Keywords*—** *MPSoC, Embedded System, Programmable Logic, Processing System, Graphical User Interface, Petalinux, GStreamer, OpenCV*

I. INTRODUCTION

Indian Space Research Organisation (ISRO) is currently involved in development of various critical technologies required to demonstrate its human spaceflight capability through its ambitious Gaganyaan mission. One of the key technology element in human spaceflight capability, is the Crew interface system. Effective crew interfaces onboard the crew module, provides the astronauts with essential information about mission parameters, environmental conditions, spacecraft status along with the ability to monitor and control various other onboard systems. In order to cater to this requirement, a compact Crew Interface and Display System (CIDS) has been designed using a Multiprocessing System on a Chip (MPSoC) processor.

Xilinx Zynq UltraScale+ MPSoC [1] is based on a heterogeneous SoC architecture. These devices integrate a high-performance quad-core ARM®-based A53 Application Processor Unit (APU), a dual-core R5 Real-Time Processing Unit (RPU), a Mali-400 Graphics Processing Unit (GPU), and a Video Codec Unit (VCU) alongside ASIC-class programmable logic. This combination enables high processing throughput and facilitates offloading of critical applications, such as graphics and video processing pipelines, to dedicated processing blocks. The integrated programmable logic further enhances performance by enabling custom hardware acceleration, resulting in significant performance gains compared to traditional processor-only solutions. Modern Space and airborne missions are pushing the boundaries of technical innovation. The ever-growing complexities of space and airborne missions necessitates powerful processing capabilities and versatile interfaces. To address this challenge a novel embedded system comprising of Zynq UltraScale+ MPSoC has been developed. This hardware integrates various high-speed interfaces like Ethernet LVDS, RS422, multi-gigabit Display Port and an audio codec. This paper details the development process of this hardware unit and its corresponding software application. The paper demonstrates the combined capabilities of the processor and programmable logic for executing both custom and standard data processing tasks.

II. HARDWARE DESIGN

The hardware leverages a mother-daughter board configuration with a high-performance COTS System-on-Module (SOM), as the motherboard. The SOM's key components include the Xilinx UltraScale+ MPSoC, 4GB of Processing System (PS) DDR4 SDRAM, 1GB of Programmable Logic (PL) DDR4 SDRAM, dual 64MB QSPI Flash devices, and 8GB of eMMC Flash. Additionally, it provides a PS reference clock input, a multi-rail power supply with a programmable power-on sequence, high-density SAMTEC make connectors for user I/Os and gigabit Ethernet interfaces. Three ultra-high-density micro header connectors serve as the primary interface between the SOM and the custom developed carrier card.

These connectors provide access to PL and PS signals, dedicated JTAG signals, system monitoring signals, a Power Management Bus (PMBUS) interface, Gigabit transceivers (GTRs), Multi-Gigabit Transceivers (MGTs), and Gigabit Ethernet. Figure-1 shows the high-level block diagram for SOM and its internal peripherals. The indigenously designed carrier card operates on a single 8V input from the Electronic Power Conditioning (EPC). Infineon multi-output Point-of-Load (POL) converters and Low-Dropout Regulators (LDOs) generate all required power rails onboard. The carrier card

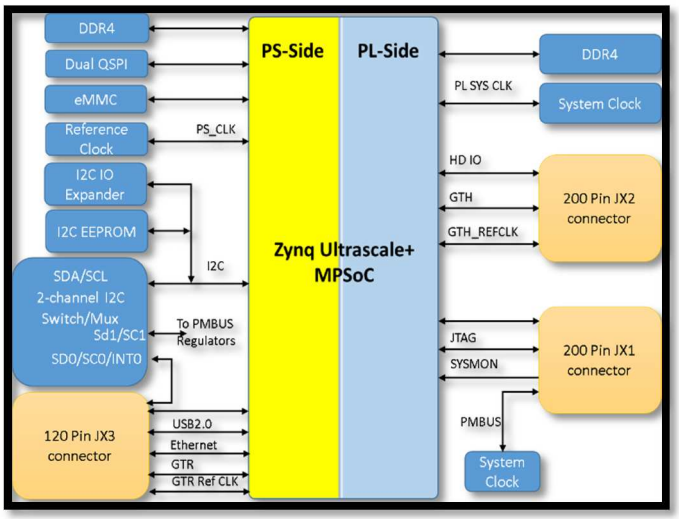

Fig.2. System on Module (SOM) high level block diagram

shown in Figure-2, utilizes three SAMTEC make micro header connectors, mirroring those on the SOM, to route various signals, including power and ground, for seamless communication with the SOM. This 20-layer carrier card PCB design [2] ensures high-density routing of all interface signals, including power and ground. Table 1 describes the system specifications.

Table 1: System Specifications

Parameter	Specifications
Core Processing Engine	XCZU7EV MPSoC • Quad Core ARM Cortex -A53 APU • Dual Core ARM Cortex R5 RPU • ARM Mali-400 GPU • Video Codec Unit(VCU) • Integrated FPGA
Memory	• Quad DDR4 in x16
Display Port Interface	Multi-gigabit transceivers
Configuration Memory Option	eMMC, QSPI NOR Flash, SD Card
Supply Voltage	8V± 0.5V,3.8A
Interface Types	I2S,I2C,LVDS,RS422,PS/PL Ethernet
Video Codec	H.264/H.265 Video enc/dec ,1080P,60fps
Dimensions	≤ 300 * 330 * 70 mm3
Total Mass	≤ 2 Kgs
Power	~ 15 W

The design leverages a subset of the available IOs on the SOM, utilizing 104 high-performance (HP) PL IOs and 48 high-density (HD) IOs for interfacing with external subsystems like Modulators-Demodulators (MODEMS), data recorders, and cameras. Appropriate drivers and receivers ensure proper electrical signaling. The multi-gigabit transceivers of the PS implements the display port interface. Additionally, a limited number of PS multiplexed I/O (MIO) pins are used for the display port auxiliary interface and specific general-purpose I/O (GPIO) functionalities, such as status signals. Due to limitations in the number of available 3.3V IOs on the MPSoC, bidirectional level translators are employed to facilitate communication with legacy 3.3V compatible devices like RS422 and LVDS drivers/receivers.

The Zynq Ultrascale+ MPSoC [3] incorporates four power domains (low-power, full-power, programmable logic, and battery) to enable power-efficient operation The CIDS application run in full power domain.The System-on-Module (SOM) receives power through the micro header connections from the carrier card. The SOM houses seven voltage regulators that generate various power rails (e.g., 0.85V, 1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V and 0.6V etc.) required for different components.

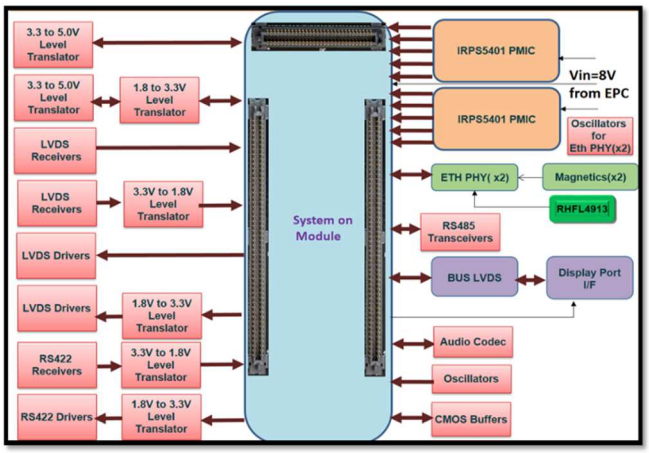

Fig.2. Carrier Card Internal Block Diagram

A precise power-up sequence is crucial to ensure the proper operation of these power rails and their corresponding power domains. To ensure a controlled power-up sequence, the hardware unit prioritizes the PS low-power (LP) domain, followed by the PS full power (FP) and PL domains. Power Management Bus (PMBus), a robust and open-standard digital communication protocol, facilitates programmable power management. Both the SOM and carrier card employ regulator ICs with a PMBus interface, typically implemented through a two-wire I2C interface. This approach enables software configuration of various power management features. One such power management regulator IC used in the design is the Infineon's IRPS5401 [4]. The IRPS5401 is a multi-output, flexible power management IC (PMIC) that integrates four high-current switching regulators (4A/2A on each two rails) and a 0.5A linear regulator within a single compact package. This multi-output capability simplifies the design and reduces the number of required components. Additionally, the IRPS5401 incorporates 64kb of one-time programmable (OTP) memory for user-specific configuration. This non-volatile memory offers data retention for up to 20 years within a wide operating temperature range (-40°C to 125°C). To address the high current demands of the MPSoC's core voltage (VCCINT), a high-current (25A) single-output buck regulator, the IR38063, is employed. This regulator also leverages on PMBus for comprehensive configuration. All PMICs used in the design has failsafe mechanism for abnormal conditions and user defined controls can be implemented. We have implemented shutdown for all the PMICs whenever any anomaly occurs.

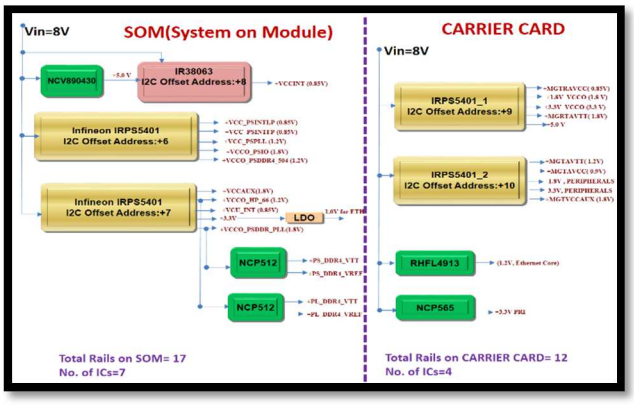

Fig. 3. Power Rails on SOM and Carrier Card

The 8V supply from the Electronic Power Conditioning (EPC) unit undergoes filtering before feeding various switching regulators on both the carrier card and SOM. Each output voltage is carefully monitored to ensure it meets specifications and adheres to the planned power-up sequence (refer to Figure 3 for the generated power rails). Once all voltage rails are verified to be within tolerance and the sequencing is confirmed, the SOM is mounted onto the carrier card. The carrier card then receives an "open-drain power good" signal from the SOM, acting as an enable signal for all its onboard regulators. Additionally, the "PS done" signal on the telemetry lines confirms a successful boot sequence. The photograph of the realized hardware is shown in Figure-4.

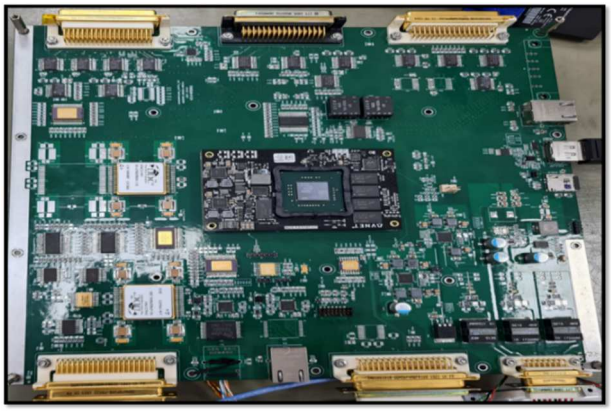

Fig. 4. SOM with Carrier Card

III. PL Software Design

The software design adopts a two-part approach: VHDL for the PL and software for the PS. Vivado design suite is used for PL based software design. These interfaces can handle various data types, including high-speed data streams (e.g. Ethernet) and slower data streams. High-speed data is transferred efficiently from the PL to the PS using Direct Memory Access (DMA). A block RAM interface with appropriate handshaking mechanisms is employed for slower data transfer. Petalinux [5], an embedded Linux development toolset, is employed as the operating system due to its streamlined integration with Xilinx hardware and device driver support. Figure 5 illustrates the data flow diagram between the PS and PL domains. As depicted in the figure, the PL interfaces with various external devices and sensors, acquiring data. This data is then transferred to the PS for further processing and control decisions. The PS can also send control signals to the PL to influence the behavior of the connected peripheral hardware units.

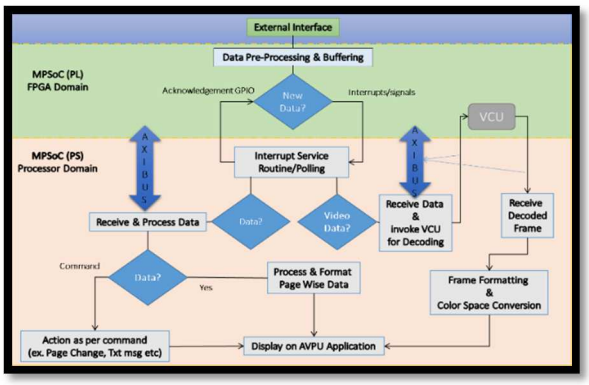

Fig. 5. Data Flow Diagram

Multiple sensors are interfaced with the hardware unit using various industry-standard protocols and interfaces, including RS422, LVDS, I2C, and UART. Whenever new sensor data such as Temperature, Pressure, Humidity, Fire, Smoke, O2 and CO2 etc. arrives in the PL from sensor controller system over LVDS interface, it is written in to the BRAM. An interrupt signal is generated to notify the PS of fresh data availability for consumption. Once the PS has processed the data, it acknowledges completion by sending a signal back to the PL through a General-Purpose Input/output (GPIO). CIDS also facilitates crew members to control various aspects of crew module such as temperature and illumination conditions by utilizing the control buttons provided in the display software. These control commands are sent to the respective controller over LVDS interface. The hardware design offers two approaches for receiving high-speed Ethernet data. The first method utilizes the processing system's integrated Ethernet controller. Alternatively, data can be received through an Ethernet physical layer (PHY) device mounted on hardware board and corresponding software implementation in the PL. Multiple event monitoring cameras, generating H.264 encoded video streams, are connected to this system. When using PS Ethernet, the received camera data is transferred to VCU within the PL for H.264 video decoding. The VCU [6] is a hardware accelerator specifically designed for efficient video processing. Decoded video frames are then made available to the PS domain through the AXI bus interface. Following the completion of the Vivado Hardware Description Language (HDL) design, the software development process commences. The generated Hardware Description File (XSA) and bit file serve as crucial inputs for creating the PS domain software application.

IV. PS Software Design

The software application (running on the PS) has dedicated pages for various mission scenarios such as ascent, descent, in-orbit, environment monitoring, avionics, communications, housekeeping and procedures. The software application

(running on the PS) has dedicated pages for various mission scenarios such as ascent, descent, in-orbit, environment monitoring, avionics, communications, housekeeping and procedures. Procedure page contains operational sequence manual for different scenarios which can be accessed by the crew when needed. All the parameters received in CIDS system has predefined threshold values which dictates the criticality levels. All the parameters are divided into three categories Normal, Warning and Caution. In normal condition all the active values are displayed in white color while in case of warning it's orange and in caution in blinking red. Based on this information crew can take possible corrective actions or can communicate to the ground operation control center.

Fig. 6. GUI- Pages for different mission scenarios

For high-speed Ethernet data received through the PS, the system leverages VCU within the PL domain to perform H.264 video decoding. The decoded video frames are then transferred back to the PS for further processing and display. The G-Streamer multimedia framework is employed to establish a software pipeline for efficient video decoding and frame reception within software application. The decoded video frames from VCU are encoded in a YUV format. To facilitate display on the GUI, these frames are converted into the RGB color space using Open-CV. Figure-6 showcases the GUI application running on the embedded system, displaying real-time data updates and video stream from the PL.

V. Performance Measurements

The hardware realization of the carrier card adopted a phased approach to ensure functionality and performance. In the initial phase, the power section was populated first, prioritizing the soldering of various Quad Flat No-Lead (QFN) devices, such as power converter ICs. Each power rail was meticulously monitored to verify that it met the specified voltage levels and adhered to the planned power-up sequence. Subsequently, the interface with the System-on-Module (SOM) was established. Critical high-speed interfaces, including the display port and Ethernet, were mounted, and signal integrity was assessed using an oscilloscope. To confirm proper protocol implementation of Ethernet PHY interface functionality, ping tests were conducted between the Ethernet PHY and the Computer. To guarantee reliable communication across all these connector pins, test clock signals were generated and monitored within various ICs. Additionally, loopback testing of these signals was performed to validate the integrity of the input paths. Once all hardware interface requirements were fulfilled, a designer-level temperature cycling test was conducted on the packaged board. Figure 7 depicts the temperature profile followed within the climatic chamber for characterizing the hardware's performance across a range of temperatures while under full PS and PL load.

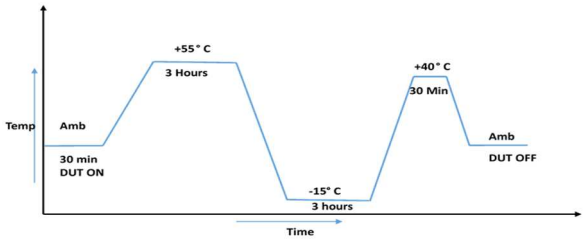

Fig. 7. Thermal Cycle Profile

The designer-level temperature cycling test yielded positive results. No hardware failures or software execution lags were observed throughout the process. The system maintained consistent performance across the temperature range, achieving a sustained video decoding and display frame rate of 60fps for 1080p resolution video. Additionally, live updates from various sensors (e.g., temperature, pressure etc.) continued to function in the background without interruption.

VI. Conclusion

The design and implementation of a state-of-the-art CIDS subsystem for ISRO's Gaganyaan mission has been elaborated in this paper. Rigorous testing was carried out across various temperature and environmental conditions to confirm the CIDS system reliability. The successful integration of programmable logic domain with a processing system enables real-time data processing and visualization through a custom-developed graphical user interface. This unique combination of features makes the system suitable for deployment in the Crew module of Gaganyaan mission. Future work may explore further optimization of the system's power consumption, more software level robustness in boot mechanism, real time operating system and customization of the graphical user interface based on feedback from astronauts.

References

[1] Zynq UltraScale+ Device Technical Reference Manual; UG1085 (v2.1) August 21, 2019
[2] UltraScale Architecture PCB Design;UG583 (v1.21)
[3] Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics; DS925 (v1.16) July 19, 2019
[4] IRPS5401 PMIC Datasheet
[5] Petalinux-Tools-Reference-Guide;UG1144(v2020.1)
[6] H.264/H.265 Video Codec Unit v1.2